AMENDMENTS TO THE CLAIMS

This Listing of Claims will replace all prior versions and listings of claims in this application.

Listing of Claims:

1. (Original) An integrated circuit for point to point simultaneous bidirectional differential high speed signalling to another integrated circuit connected thereto, the integrated circuit comprising:

a transmitter for transmitting a first signal to another integrated circuit,~~;~~ wherein the transmitter having a ~~an output~~ transmitter buffer;

a receiver for receiving a second signal from the other integrated circuit, wherein the receiver having a receiver buffer and co-located on the same integrated circuit; and

a differential buffer coupled between the input of the transmitter buffer and the output of the receiver buffer,~~;~~

wherein the first signal at the output of the transmitter buffer is coupled into the input of the receiver buffer co-located on the same integrated circuit,~~; and~~

wherein a third signal at the input of the transmitter buffer is passed through the differential buffer and coupled onto the output of the receiver buffer;

wherein the differential buffer adjusts the third signal in phase and amplitude to cancel the first signal at the output of the receiver buffer, whereby the quality of receiving the second signal is enhanced by canceling echoing of the first signal.

2. (Original) The integrated circuit according to claim 1, wherein the third signal is further adjusted in rise time.

3. (Original) The integrated circuit according to claim 1, wherein the gain and phase of the differential buffer is varied by means of a finite state machine using a training pattern following power up or on request.

4. (Original) The integrated circuit according to claim 1, wherein the differential buffer is implemented as a chain of buffer stages.

5. (Original) The integrated circuit according to claim 1, wherein the finite state machine employs a peak detector and means of reading a parameter related to the peak detector to set a value through digital to analogue converters which controls the currents sources in the differential stages in the chain of buffers providing the third signal between the transmitter and receiver.

6. (Original) The integrated circuit according to claim 1, wherein the differential buffer has a variable current source for the purpose of setting the amplitude or phase of the third signal.

7. (Original) The integrated circuit according to claim 1, wherein the differential buffer has a programmable or variable load which is set by a finite state machine following a training pattern initiated after power up or on request.

8. (Original) The integrated circuit according to claim 1, wherein the differential buffer includes a coarse delay circuit, a fine delay circuit, an amplitude control circuit and a rise-time control circuit controlled by a finite state machine.

9. (Original) The integrated circuit according to claim 8, wherein the output amplitude, phase and rise-time of the differential buffer is varied by means of a finite state machine using a training pattern following power up or on request.

10. (Original) The integrated circuit according to claim 9, wherein the finite state machine employs a peak detector and means of reading a parameter related to the peak detector, the parameter being used to set a value through a digital to analogue converter and digital control signals to set the amplitude, phase and rise-time of the third signal between the transmitter and receiver.

11. (Original) The integrated circuit according to claim 8, wherein the coarse delay circuit comprises a digital delay line, a pair of multiplexers and logic for control of the multiplexers.

12. (Original) The integrated circuit according to claim 9, wherein the digital delay line comprises a cascade of buffers.

13. (Original) The integrated circuit according to claim 9, wherein a pair of multiplexers selects signals from the digital delay line.

14. (Original) The integrated circuit according to claim 9, wherein a finite state machine generates control signals to select the signals from the digital delay line in the coarse delay circuit varying the delay of the third signal with respect to the first signal.

15. (Original) The integrated circuit according to claim 9, wherein a finite state machine generates control signals to select the signals from the delay circuits in the fine delay circuit varying the delay of the third signal with respect to the first signal.

16. (Original) The integrated circuit according to claim 1, wherein the coarse delay circuit is cascaded with the fine delay circuit to produce a delay circuit with a wide range and high resolution.

17. (Original) The integrated circuit according to claim 1, wherein a finite state machine plus ADC generates the control voltage to vary the amplitude of the third signal.

18. (Original) The integrated circuit according to claim 8, wherein the amplitude control circuit comprises a buffer with a variable load.

19. (Original) The integrated circuit according to claim 18, wherein the variable load comprises a NMOS transistor whose gate voltage and therefore resistance is controlled by the finite state machine.

20. (Original) The integrated circuit according to claim 9, wherein the rise-time control circuit comprises switches, capacitors and control logic.

21. (Original) The integrated circuit according to claim 9, wherein a finite state machine generates control signals to switch the capacitors in the rise-time control circuit varying the rise-time of the third signal.

22. (Original) The integrated circuit according to claim 16, wherein the peak detector comprises an amplitude cancellation sensor, a phase cancellation sensor and an analogue multiplexer.

23. (Original) The integrated circuit according to claim 4, wherein the state machine controls the amplitude and/or phase adjustment on power up or on request, sequentially, first the master and then the slave.

24. (Original) The integrated circuit according to claim 23, wherein the amplitude cancellation sensor comprises an integrator plus a sample and hold device.

25. (Original) The integrated circuit according to claim 24, wherein the timing of the phases for the integrator includes a reset phase, an integration phase and a transfer phase.

26. (Currently amended) The integrated circuit according to claim 25, ~~wherein the~~ timing of the phases for the ~~amplitude~~ phase sensor is controlled by the finite state machine.

27. (Original) The integrated circuit according to claim 1, wherein patterns are injected into the transmitter for the purpose of measuring the offset in the amplitude cancellation sensor.

28. (Original) The integrated circuit according to claim 22, wherein the phase cancellation sensor comprises a full-wave rectifier plus integrator and a sample and hold.

29. (Original) The integrated circuit according to claim 24, wherein the integrator includes a reset phase, an integration phase and a transfer phase.

30. (Original) The integrated circuit according to claim 28, wherein the timing of the phases for the phase cancellation sensor is controlled by the finite state machine.

31. (Canceled).

32. (Original) The integrated circuit according to claim 5, wherein multiple patterns are selectable by the finite state machine for the purposes of offset calibration, amplitude cancellation, phase cancellation and rise-time cancellation.

33. (Original) The integrated circuit according to claim 1, wherein either the differential buffer or the output buffer of the transmitter is adapted to be switched off with the effect that the first signal is not canceled but is passed to the receiver for testing purposes.

34. (Original) The integrated circuit according to claim 1, wherein the load in the differential buffer providing the third signal is implemented as N-type FET transistors to minimise the parasitic capacitance.

35. (Original) A method for echo cancellation in simultaneous bidirectional differential high speed signalling, where the signalling is from one integrated circuit connected to another integrated circuit, each circuit comprising a transmitter having an output buffer and a receiver having a receiver buffer; the method comprising: transmitting a first signal from the output buffer of the transmitter arranged on one integrated circuit, to another circuit, the first signal being coupled also into the input buffer of the receiver co-located with the transmitter on the same integrated circuit; receiving a second signal from the other integrated circuit; transmitting a third signal from the input of the transmitter buffer through a differential buffer where the third signal is adjusted in phase and amplitude; and coupling the adjusted signal onto the output of the

receiving buffer to cancel the first signal, whereby the quality of receiving the third signal is enhanced by canceling echoing of the first signal.

36. (Original) A method according to claim 35, wherein the phase of the third signal applied to the output of the receiving buffer is opposite to the phase of the first signal.

37. (Original) A method according to claim 35, wherein the rise time of the third signal applied to the output of the receiving buffer is adjusted to match the rise time of the first signal.

38. (Original) A method according to claim 35 wherein the gain of the differential buffer is varied by means of a finite state machine using a training pattern.

39. (Original) A method according to claim 35 wherein the phase and/or amplitude of the third signal is adjusted by applying a training pattern and minimising peak to peak noise by varying the codes in DACs, measuring noise using a peak detector and ADC to determine which code corresponds to the minimum noise using state machine and applying the determined code to the DACs at the end of adjustment process.

40. (Original) A method according to claim 35 wherein one of the circuits is a master die and another is a slave die, while the determining is repeated twice, first to configure the master die, and second to configure the slave die.